Abstract of the Disclosure

A signal processing integrated circuit has having a chopper stabilized, multistage, feedforward amplifier and a delta sigma analog to digital converter. Filtering of the output of the output from the analog to digital converter comprises a $sinc^5$ filter and a $sinc^3$ filter. The $sinc^3$ filter may be bypassed. A rough buffer permits quick charging of a sample and hold capacitor during part of the charge cycle and slower but more accurate charging during the remainder of the charge cycle.